



2825 12/1/01

**PATENT APPLICATION  
ATTORNEY DOCKET NO. Q56320**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Kaoru NARITA

Appln. No.: 09/421,273

Group Art Unit: 2823

Confirmation No.: Not Yet Assigned

Examiner: J. Garcia

Filed: October 20, 1999

For: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED  
BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT  
AND PROCESS OF FABRICATION

**SUBMISSION OF FORMAL DRAWINGS**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Submitted herewith please find eleven (11) sheets of Formal Drawings. The submitted  
Formal Drawings are identical to the drawings submitted to the Patent Office on October 20,  
1999, and no new matter has been incorporated into the Formal Drawings. The Examiner is  
respectfully requested to acknowledge receipt of these Formal Drawings.

Respectfully submitted,

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Date: November 30, 2001

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